

for the SIA Family

## **Continuous Rate Clock Recovery**

For accurate and repeatable measurements when access to a bit clock is not available

The addition of a Continuous Rate Clock Recovery option to an SIA solution enables signal integrity analysis and diagnostics measurements when access to a bit clock is not available. This option is especially useful for applications with non-standard data rates. The Continuous Rate Clock Recovery option removes the need for awkward setups; simply plug in your test signal and you can obtain accurate and repeatable measurements. Eye diagrams and detailed jitter analysis can be performed on any type of data signal - random or repeating.

## **Clock Recovery Setup**

The Continuous Rate Clock Recovery option is used as follows:

Data from the DUT is sent into the Continuous Rate Clock Recovery option via the "Data In" channel on the front of the SIA solution. The supplied Hard-line SMAs are used to connect from the Continuous Rate Clock Recovery "Data Out" to the IN1 (Channel 1 input). The recovered clock is used internally for all signal integrity measurements.



## **Specifications**

Data Rates30 Mb/s tp 3 Gb/sPLL Loop BandwidthDatabaud /1244 Typical

Clock Jitter\*

Databaud < 500 Mb/s < 5.0ps RMS
Databaud > 500 Mb/s < 3.0ps RMS
Insertion Loss Through Path 8 dB Typical

**Operating Input Signal Level** 

Single Ended 0.250 to 2.5 Volts (pk-pk)
Differential 0.125 to 1.25 Volts (pk-pk)

## **Benefits:**

Enables measurement of any data signal - random or repeating

Supports multiple data rates and applications:

PCI Express Gen I and Gen II Fibre Channel: IX, 2X, 3X, 4X

SAS & SATA: 1.5, 3.0

Gigabit Ethernet

Infiniband SONET

JOINLI

OC-3,12,48

**XAUI** 

10GFC

Serial RapidIO

DVI

1394b: 800 Mb/s, I.6 Gb/s

Fast Ethernet

**HDMI** 

Custom: 30 to 3000 Mb/s

Easy setup - simply plug in test signal

SIACR DS001\_R1

<sup>\*</sup>Measured using PRBS 2^23-1 test pattern